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INFORMATION DISCLOSURE CITATION (Use several sheets if necessary)							
				Applicant(s) BONG-JOON LEE, et al.			
				Filing Date Herewith	Group Unknown		
U.S. PATENT DOCUMENTS							
*Examiner Initials		Document Number	Date	Name	Class	Subclass	Filing Date
	AA						
FOREIGN PATENT DOCUMENTS							
*Examiner Initials		Document Number	Date	Country	Class	Subclass	Translation YES NO
	AB						
OTHER DOCUMENTS							
/JJ/	AC	Savoj, J. et al., "A 10-Gb/s CMOS Clock and Data Recovery Circuit with a Half-Rate Linear Phase Detector" <u>IEEE Journal of Solid-State Circuits</u> , Vol. 36, No. 5, May 2001, pages 761-767.					
/JJ/	AD	Lee, Sang-Hyun, et al., "A 5Gb/s 0.25μm CMOS Jitter-Tolerant Variable-Interval Oversampling Clock/Data Recovery Circuit," <u>2002 IEEE International Solid-State Circuits Conference</u> , Digest of Technical Papers, pages 256-257 and 465 (February 2002).					
/JJ/	AE	Moon, Yongsam, et al., "A 0.6 – 2.5Gbaud CMOS Tracked 3x Oversampling Transceiver with Dead-Zone Phase Detection for Robust Clock/Data Recovery," <u>2001 IEEE International Solid-State Circuits Conference</u> , Digest of Technical Papers, pages 212-213 and 448 (February 2001).					
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/JJ/	AG	Fiedler, A., et al., "A 1.0625Gbps Transceiver with 2x-Oversampling and Transmit Signal Pre-Emphasis," <u>1997 IEEE International Solid-State Circuits Conference</u> , Digest of Technical Papers, pages 238-239 (February 1997).					
/JJ/	AH	Larsson, Patrik, "A 2-1600-MHz CMOS Clock Recovery PLL with Low-Vdd Capability," <u>IEEE Journal of Solid-State Circuits</u> , Vol. 34, No. 12, December 1999, pages 1951-1960.					
Examiner /Jaison Joseph/				Date Considered 03/29/2007			
* Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							